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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,287	04/14/2005	Tadaaki Tanimoto	TAM-103	4868

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EXAMINER	
PARIHAR, SUCHIN	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/531,287	TANIMOTO ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *6-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to application 10/531,287, filed 4/14/2005. Claims 1-20 are pending in this application.

Election/Restrictions

1. Claims 1-5, drawn to a compiler with a conversion program and without a first step which inputs first program descriptions which contain register assignment statements.

2. Claims 6-20, drawn to a logic circuit design method with a first step which inputs first program descriptions which contain register assignment statements and without conversion program.

3. This application contains claims directed to the following patentably distinct species: Groups I and II. The species are independent or distinct for the reasons given above in paragraphs 1 and 2 of the office action.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

4. During a telephone conversation with John R. Mattingly (Reg.# 30,293) on 9/6/2006 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-5. Affirmation of this election must be made by applicant in replying to this Office action. Claims 6-20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Information Disclosure Statement

5. The information disclosure statement filed 4/14/2005 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

With regard to the IDS filed 4/14/2005, Applicants' fail to supply the references AT, AU and AV listed on the IDS. Therefore, these references have not been considered.

Also, references AP and AQ do not cite the publication date, or at least the publication year, on the IDS. Therefore, these references have not been considered.

6. The following paragraph pertains to the PCT Search report, which was submitted, but was not listed on the IDS as a separate NPL document:

> The listing of references in the Search Report is not considered to be an information disclosure statement (IDS) complying with 37 CFR 1.98. **37 CFR 1.98(a)(2) requires a legible copy of: (1) each foreign patent; (2) each publication or that portion which caused it to be listed;** (3) for each cited

pending U.S. application, the application specification including claims, and any drawing of the application, or that portion of the application which caused it to be listed including any claims directed to that portion, unless the cited pending U.S. application is stored in the Image File Wrapper (IFW) system; and (4) all other information, or that portion which caused it to be listed. In addition, each IDS must include a list of all patents, publications, applications, or other information submitted for consideration by the Office (see 37 CFR 1.98(a)(1) and (b)), and MPEP § 609.04(a), subsection I. states, "the list ... must be submitted on a separate paper." Therefore, the references cited in the Search Report have not been considered. Applicant is advised that the date of submission of any item of information or any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the IDS, including all "statement" requirements of 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Objections

7. Claim 3 is objected to because of the following informalities: In claim 3, line 19, the phrase "the circuit descriptions" lacks antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. **Claims 1-5 are rejected under 35 U.S.C. 102(e)** as being anticipated by Tojima (US PG Pub 2003/0005392).

10. With respect to claim 1, Tojima teaches a compiler (i.e. build-in C compiler, paragraph [0004]) comprising:

a conversion program (i.e. converting an algorithm C description, paragraph [0012]);

wherein the conversion program can convert first program descriptions (i.e. converting an algorithm C description, paragraph [0012]) described by diverting a predetermined program language (i.e. C programming language, paragraph [0012]) into circuit descriptions (i.e. converting the functional C description into a RTL level C description, paragraph [0012]);

the first program descriptions contain register assignment statements (i.e. assignment of data to parameters correspond to register parts, paragraph [0092]) with particular operators (i.e. operator such as a multiplier, paragraph [0104]) and clock boundary descriptions (i.e. clock level descriptions, paragraph [0004]), and which permit circuit operations to be specified at a cycle precision (i.e. the execution cycle of each state can be estimated by inserting a clock counting function which enables estimation of processing performance with high precision, paragraph [0017]); and

the circuit descriptions specify hardware realizing the circuit operations (i.e. converting an algorithm C language into a functional C description describing control of hardware, paragraph [0012]) specified by the first program descriptions (i.e. RT level C description, paragraph [0012]) in a predetermined hardware description language (RTL, paragraph [0012]).

11. With respect to claim 4, Tojima teaches all the elements of claim 1, from which the claim depends. Tojima teaches: wherein the predetermined program language is a C language (i.e. C descriptions, paragraph [0012], also see Fig 1).

12. With respect to claim 5, Tojima teaches all the elements of claim 1, from which the claim depends. Tojima teaches: wherein the hardware description language is a description language of RTL level (i.e. RT level C description, paragraph [0012]).

13. With respect to claim 2, Tojima teaches a compiler (i.e. build-in C compiler, paragraph [0004]) comprising:

a conversion program (i.e. converting an algorithm C description, paragraph [0012]);

wherein the conversion program can convert first program descriptions (i.e. converting an algorithm C description, paragraph [0012]) described by diverting a predetermined program language (i.e. C programming language, paragraph [0012]) can be converted into second program descriptions (i.e. converting into a functional C description, paragraph [0012]) using a predetermined program language (i.e. C programming language, see abstract or paragraph [0012]);

the first program descriptions contain register assignment statements (i.e. assignment of data to parameters correspond to register parts, paragraph [0092]) with particular operators (i.e. operator such as a multiplier, paragraph [0104]) and clock boundary descriptions (i.e. clock level descriptions, paragraph [0004]), and which permit circuit operations to be specified at a cycle precision (i.e. the execution cycle of each state can be estimated by inserting a clock counting function which enables estimation of processing performance with high precision, paragraph [0017]); and

the second program descriptions contain transformed assignment statements into which the register assignment statements are transformed () in order to make states of preceding cycles referable (i.e. returning to the unit of processing A, paragraph [0061]), and register assignment description insertion statements (i.e. inserting a clock description in the functional C description to convert the functional C description into the RT level description, paragraph [0012]) which associate variables of the transformed assignment statements with changes of registers attendant upon cycle changes (i.e. functions are expressed in a language using a register as a variable, in the form of a clock level simulator, paragraph [0003], Examiner notes that this limitation is interpreted as follows: changes in a register leads to a change to its variable), in correspondence with the clock boundary descriptions (i.e. clock level descriptions, paragraph [0004]).

14. With respect to claim 3, Tojima teaches a compiler (i.e. build-in C compiler, paragraph [0004]) comprising:

a conversion program (i.e. converting an algorithm C description, paragraph [0012]);

wherein the conversion program can convert first program descriptions (i.e. converting an algorithm C description, paragraph [0012]) described by diverting a predetermined program language (i.e. C programming language, paragraph [0012]) into second program descriptions (i.e. converting into a functional C description, paragraph [0012]) using a predetermined program language (i.e. C programming language, see abstract or paragraph [0012]);

the first program descriptions contain register assignment statements (i.e. assignment of data to parameters correspond to register parts, paragraph [0092]) with particular operators (i.e. operator such as a multiplier, paragraph [0104]) and clock boundary descriptions (i.e. clock level descriptions, paragraph [0004]), and which permit circuit operations to be specified at a cycle precision (i.e. the execution cycle of each state can be estimated by inserting a clock counting function which enables estimation of processing performance with high precision, paragraph [0017]);

the second program descriptions contain transformed assignment statements into which the register assignment statements are transformed () in order to make states of preceding cycles referable (i.e. returning to the unit of processing A, paragraph [0061]), and register assignment description insertion statements (i.e. inserting a clock description in the functional C description to convert the functional C description into the RT level description, paragraph [0012]) which associate variables of the transformed assignment statements with changes of registers attendant upon

cycle changes (i.e. functions are expressed in a language using a register as a variable, in the form of a clock level simulator, paragraph [0003], Examiner notes that this limitation is interpreted as follows: changes in a register leads to a change to its variable), in correspondence with the clock boundary descriptions (i.e. clock level descriptions, paragraph [0004]); and

the circuit descriptions specify hardware (i.e. a functional C description describing control of hardware, paragraph [0012]) which is defined by the second program descriptions, in a predetermined hardware description language (RTL description, paragraph [0012]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Suchin Parihar
Examiner
AU 2825

PAUL DINH
PRIMARY EXAMINER